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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/773,520 | 02/05/2004 | Joseph M. Jeddeloh | 33583/US | 6540 |

7590 03/29/2006

Edward W. Bulchis, Esq.
DORSEY & WHITNEY LLP
Suite 3400
1420 Fifth Avenue
Seattle, WA 98101

| EXAMINER | |
|---|---|
| DOAN, DUC T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2188 | |

DATE MAILED: 03/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/773,520 | JEDDELOH, JOSEPH M. | |
| | Examiner | Art Unit | |
| | Duc T. Doan | 2188 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Status of Claims*

Claims 1-33 are in the application.

Claims 1-33 are rejected.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11,13-17,19-24,27-33 rejected under 35 U.S.C. 103(a) as being unpatentable over Desota et al (US 2005/0149603) and in view of Osborne (US 2003/0156581).

As in claim 1, Desota describes a memory hub (Fig 4: #120), comprising: a decoder being operable to receive memory requests and to determine a memory request identifier associated with each memory request (Desota's Fig 6: #102, #104); a packet memory coupled to the decoder, the packet memory being operable to receive memory request identifiers from the decoder and to store the received memory request identifiers (Desota's Fig 6: #106' the new

transaction is stored in a link list behind early transaction; paragraphs 22, 32 further describes the current transactions and new transactions or "requests" are stored in queues/registers #502 #506 #520 that corresponds to the claim's packet memory); a packet tracker coupled to the packet memory, the packet memory being operable to receive remote memory responses and to associate each received remote memory response with a memory request identifier stored in the packet memory ( Desota's Fig 6: #102) , the packet tracker being operable to cause the memory request identifier to be effectively removed from the packet memory (Desota's Fig 6: #108; paragraph 34); a multiplexor being operable to couple either the received remote memory responses or the local memory responses to an output responsive to a control signal; and arbitration control logic coupled to the multiplexor and the packet memory and being operable to generate the control signal (Desota's Fig 8, paragraphs 37-39 describes the remote transaction is saved and latter selected for processing based on its priority, therefore Desota clearly suggest that multiplexer and arbitration circuits must be employed for switching from completing a previous transaction in the local node to begin processing the remote transaction ). Desota does not describe the claim's aspect of memory utilizing the packet transactions. However, Osborne teaches a modern hub based memory system in which the hubs (Fig 1: #104, #106) connect various components via point-to-point packet links. It would have been obvious to one of ordinary skill in the art at the time of invention to include memory interconnect links and methods as suggested by Osborne in Desota's system thereby providing a mechanism to transfer data with much higher bandwidth and maintaining a narrow interface (Osborne's paragraphs 4,22).

As for claims 2-3, the claims recite wherein the arbitration control logic generates the control signal based on an oldest memory request identifier in the packet memory (claim 2); wherein the packet memory is a first-in, first-out (FIFO) memory. Desota's Fig 6 clearly shows the transactions are queued in a linked list and processed based on the oldest entries in the link list.

As in claim 4, the claim recites wherein the arbitration control logic generates the control signal such that if an oldest memory request in the packet memory is a local memory request, the multiplexor outputs a local memory response. Desota's Fig 6 and paragraphs 28-30 describes a situation in which the current transaction is processed locally, and when it completed, the response or result will be send back to the requestor, thus obviously, the multiplexer must select the output connecting to the response or result of the transaction processed locally.

As in claim 5, the claim recites wherein each of the local and remote memory responses comprise data and a header identifying a memory request corresponding to the memory response. It has been known a packet comprises data and header information to identifying the source and other attributes, and the associating memory address. Osborne shows such a packet in figs 4-8.

As in claim 6, the claim recites a memory hub being operable to receive local memory responses and remote memory responses, the memory hub being operable to store the received memory responses and to apply an arbitration algorithm to select the order in which the stored local and remote memory responses are provided on an uplink output based on the ages of memory requests corresponding to the stored local and remote memory responses. The claim rejected based on the same rationale as in the rejection of claim 1.

Claims 6,11,17,24,29 rejected based on the same rationale as in the rejection of claim 1.

As in claim 7, the claim recites wherein the memory hub further comprises a packet memory that stores memory request identifiers in an order in which the corresponding memory requests are received. Desoto's Fig 6, paragraphs 31-32 shows the link list, and associating registers/queues to store transactions that were received.

As for claims 8-9, the claims recite wherein the memory hub further comprises a multiplexer coupled to the packet memory, the multiplexor providing either a local or a remote memory response on an output responsive to a control signal (claim 8); wherein the memory hub further comprises arbitration logic coupled to the packet memory and the multiplexer, and wherein the arbitration logic applies the control signal to the multiplexer to control which memory responses are provided on the output (claim 9). The claims rejected based on the same rationale as in the rejection of claim 1.

Claim 10,16,23,28,30,36 rejected based on the same rationale as in the rejection of claim 5.

Claims 13,19,31 rejected based on the same rationale as in the rejection of claim 2.

Claims 14,22,32 rejected based on the same rationale as in the rejection of claim 3.

Claims 15,20-21,33 rejected based on the same rationale as in the rejection of claim 4.

As in claim 27, Desota's Fig 3 describes wherein the processor comprises a central processing unit (CPU).

Claims 18,25 rejected under 35 U.S.C. 103(a) as being unpatentable over Desota et al (US 2005/0149603), Osborne (US 2003/0156581) as applied to claims 17,24, and in view of Woodruff et al (US 2005/0015426).

As in claim 18, the claim recites wherein each of the high-speed links comprises an optical communications link. Desota does not describe the claim's aspect of optical link. However, Woodruff teaches optical link are employed in various memory hubs (Woodruff's paragraph 34). It would have been obvious to one of ordinary skill in the art at the time of invention to include optical communication link as suggested by Woodruff in Desota's system thereby further increase the data transfer rate over a communication link due to high frequency provided by optical signal (Woodruff's paragraphs 4-5).

Claim 25 rejected based on the same rationale as in the rejection of claim 18.

Claims 12,26 rejected under 35 U.S.C. 103(a) as being unpatentable over Desota et al (US 2005/0149603), Osborne (US 2003/0156581) as applied to claims 11,24, and in view of Zumkehr et al (US 6901494).

As in claim 12, the claim recites wherein each of the memory devices comprise SDRAMs. Desota does not describe the claim's aspect of SDRAM memory. However, Zumkehr teaches a memory controller translator circuit capable of converting memory access commands of a packet-based interface (rambus interface) into sdram interface for accessing data in sdram devices. It would have been obvious to one of ordinary skill in the art at the time of invention to include the memory controller translator circuit as suggested by Zumkehr in Desota's system thereby further allowing to use commonly off the shelf high density dram memory devices in a high-speed point-to-point interface such as rambus, and achieving high utilization of the memory bus (Zumkehr's column 2 lines 1-25).

Claim 26 rejected based on the same rationale as in the rejection of claim 12.

*Conclusion*

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kapur et al (US 6912617).

Zimmerman (US 2005/0105350).

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 3/20/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER

DD

Mano Padmanabhan

Supervisory Patent Examiner

TC2188